ABSTRACT

A process for enhancing refresh in Dynamic Random Access Memories wherein n-type impurities are implanted into the capacitor buried contact after formation of the access transistor components. The process comprises forming a gate insulating layer on a substrate and a transistor gate electrode on the gate insulating layer. First and second transistor source/drain regions are formed on the substrate adjacent to opposite sides of the gate electrodes. N-type impurities, preferably phosphorous atoms, are then implanted into the first source/drain region which will serve as the capacitor buried contact.